WHAT IS CLAIMED IS:

Sub B2

1. A device for detecting a fixed pattern, said device being fed as a received signal with a pattern of a length of N chips, said received signal being obtained on dividing and re-arraying each of K symbols in terms of a chip period as a unit, K being a preset positive integer, each of said symbols being spread with a spread code at a rate of M chips per symbol, M being a preset positive integer, and on repeatedly inserting into the re-arrayed symbols a signature pattern of a length K having one chip period as a unit, by M times, where N=K×M, said signature pattern being detected from said received signal,

said device comprising:

first-stage correlators taking correlation between M received signals spaced apart from one another by every K chips, and M spread code sequences obtained on jumping a spread code sequence of a length N by every Kth chip to output correlation values associated with K signatures, respectively; and

a second-stage correlators taking correlation between the correlation values associated with K signatures output by said first-stage correlators and a pre-defined signature pattern.

2. The fixed pattern generator as defined in claim 1

wherein

said first-stage correlators are each fed with a spread code sequence of a length M obtained on decimating and re-arraying a spread code sequence of a length L generated by a

spread code generator at every K chips and classifying the re-arrayed sequence into K to output correlation values associated with K signatures.

3. The fixed pattern generator as defined in claim 2 wherein

said correlators make up K correlator blocks;

each of said K correlator blocks is made up of a plurality of (R+1) correlators of a length M arranged in parallel with one another;

in each of the correlator blocks, the first correlator of said (R+1) correlators is fed with M received signals every K chips and said spread code sequence to take correlation of a length M, the second correlator is fed with M received signals, at every K chips, having the received signal supplied to said correlator as second data, as leading end data, and with a spread code sequence which is said spread code sequence supplied to said first correlator delayed by a delay element in synchronism with an operating period, to take correlation with a length equal to M, and so on, such that the (R+1)st correlator is fed with M received signals at every K chips, having the received signal supplied to said correlator as second data, as leading end data, and with a spread code sequence which is said spread code sequence supplied to said first correlator and delayed by R delay elements in synchronism with an operating period, to take correlation with a length equal to M.

4. The fixed pattern detection device as defined in claim 2 in which, in calculating correlation values shifted chip by chip for N+L chips, where L, which is an integer divisible by K, denotes an indefinite time range where there exists said signature pattern;

wherein

each of said K correlator blocks has L/K+1 correlators of a length M, arranged in parallel.

5. The fixed pattern detection device as defined in claim 2 in which, in calculating correlation values shifted chip by chip for N+L chips, where L, which is an integer divisible by K, denotes an indefinite time range during which there exists said signature pattern;

wherein

each of said K correlator blocks has L/(n×K)+1 correlators of a length M, arranged in parallel, where n is an integer not less than 2 provided that L is divisible by n×K.

6. A device for detecting a fixed pattern, said device being fed as a received signal with a pattern of a length of N chips, said received signal being obtained on dividing and re-arraying each of a plurality of or K symbols in terms of a chip period as a unit, each said symbols being spread with a spread code at a rate of M chips per symbol, M being a preset positive integer, and on repeatedly inserting into the re-arrayed symbols a signature pattern of a length K having one chip period as a unit, by M times,

where N=K×M, said signature pattern being detected from said received signal,

said device comprising:

(a) a received signal storage memory transiently storing received signals for at least N+L chips where L, which is an integer divisible by K, denotes an indefinite time range during which there exists said signature pattern;

(b) a spread code generator generating a spread code;

(c) a spread code re-arraying unit jumping and re-arraying the spread code generated by said spread code generator;

(d) a received signal storage memory controller controlling readout from said received signal storage memory;

(e) first-stage correlators comprised of K juxtaposed correlator blocks, each block being of an M chip length;

(f) K spread code shift registers storing the spread code sequence re-arrayed by said spread code re-arraying unit to shift-output said spread code sequence to said K correlator blocks, respectively, of said first-stage correlators;

(g) each of said correlator blocks of said first-stage correlators being fed with a spread code sequence from said spread code shift register associated with each of said correlator blocks, each of said correlator blocks outputting a correlation value of the received signal read out from said received signal storage memory and said spread code sequence;

(h) a correlation value storage memory storing the

correlation value output from said first stage correlators;

(i) a correlation value storage memory controller controlling writing of the correlation value output from the first-stage correlators and reading-out of the correlation value from said received signal storage memory;

(j) a signature pattern storage unit storing and holding a preset signature pattern;

(k) second-stage correlators calculating correlation values between the correlation values read out from said correlation value storage memory controller and said signature pattern stored in said signature pattern storage unit; and

(l) a signature detector detecting the signature from the correlation value output from said second-stage correlators to output a fixed pattern detection signal.

7. The fixed pattern detection device as defined in claim 6 in which, in calculating correlation values shifted chip by chip for N+L chips, where L, which is an integer divisible by K, denotes an indefinite time range during which there exists said signature pattern; said fixed pattern detection device having L/K+1 correlators arranged in a juxtaposed fashion, each with a length equal to M,

wherein

said correlators are arrayed in blocks, and

in each of the correlator blocks, the first correlator of said L/K+1 correlators is fed with M received signals read out

from said received signal storage memory, at every K chips, and said spread code sequence, to take correlation of a length M;

the second correlator is fed with M received signals, at every K chips, having the received signal as supplied to said correlator as second data, as leading end data, and with a spread code sequence which is said spread code sequence supplied to said first correlator delayed by a delay element in synchronism with an operating period, to take correlation with a length equal to M;

and so on;

such that the L/K+1st correlator is fed with M received signals at every K chips, having the received signal as supplied to the L/Kth correlator as second data, as leading end data, and with a spread code sequence which is said spread code sequence supplied to said first correlator and delayed by L/K delay elements in synchronism with an operating period, to take correlation with a length equal to M.

8. The fixed pattern generator as defined in claim 6

wherein

each said K correlator blocks is made up of a plurality of (R+1) correlators, each of a length M, arranged in parallel with one another;

in each of said correlator blocks, the first correlator of said (R+1) correlators is fed with M received signals at every K chips and said spread code sequence as read out from said

received signal storage memory to take correlation of a length M;

the second correlator is fed with M received signals, at every K chips, having the received signal as supplied to said correlator as second data, as leading end data, and with a spread code sequence which is said spread code sequence supplied to said first correlator from the spread code register and delayed by a delay element in synchronism with an operating period, to take correlation with a length equal to M;

and so on;

such that the (R+1)st correlator is fed with M received signals at every K chips, having the received signal supplied to said Rth correlator as second data, as leading end data, and with a spread code sequence which is said spread code sequence supplied to said first correlator and delayed by R delay elements in synchronism with an operating period, to take correlation with a length equal to M.

9. The fixed pattern generator as defined in claim 8

wherein

each of said K correlator blocks has L/(n×K)+1 correlators arranged in parallel, where n is such an integer which is not less than 2 and which renders L divisible by n×K.

10. The fixed pattern detection device as defined in claim 8 in which, in calculating correlation values shifted chip by chip for N+L chips, where L, which is an integer divisible by K, denotes an L chip range that is an indefinite time range during

which there exists said signature pattern, processing of calculating the correlation values in said K correlator blocks is repeated for each received signal belonging to a section obtained on dividing said L into plural portions, to obtain correlation values in an N+L chip range.

11. The fixed pattern detection device as defined in claim 6 wherein

a plurality said second stage correlators are provided in association with plural sorts of said signature patterns.

12. The fixed pattern detection device as defined claim 6 wherein

said spread code re-arraying unit is configured for variably re-arraying the spread code generated in said spread code generator responsive to the re-arraying state of said signature pattern for distribution to said plural spread code shift registers.

13. A CDMA reception apparatus having the fixed pattern detection device as defined in any one of claim 1.

14. In a spread spectrum communication apparatus, a detection device for detecting a signature pattern from said received signal, said detection device being fed as an input a received signal with a pattern of a length of N chips, into which is repeatedly inserted M times a signature pattern of a length K with a one-chip period as a unit, said signature pattern, being obtained on dividing and re-arraying each signature of K symbols

each being spread with the spread code at a rate of M chips per symbol,

said device in the spread spectrum communication apparatus comprising:

first-stage correlators taking correlation between M received signals spaced apart from one another at every K chips, and M spread code sequences obtained on decimating a spread code sequence of a length N at every K chips to output correlation values associated with K signatures; and

second-stage correlators taking correlation between the correlation values associated with K signatures output by said first-stage correlators and a pre-defined signature pattern.